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# Purpose of Today's Meeting:

# Keep Everyone Informed

- **ADTV Overview** — **Glenn**
- **Comments** — **Curt**
- **Integration Plan** — **Norm**
- **Making It Happen** — **Glenn**
- **Concluding Remarks** — **Jim**

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# The Great Race

- **There are four digital HDTV systems under consideration:**
  - DigiCipher (GI/MIT)
  - Digital Spectrum Compatible-HDTV (Zenith/AT&T)
  - ADTV (ATRC = DSRC, TCE, NAP, NBC, CLI)
  - ATA-Progressive (MIT/GI)

- **We now have much more detail on DigiCipher and DSC-HDTV**
  - ATA-Progressive will use DigiCipher transmission

- **ADTV can win!!**
  - picture quality
  - coverage area
  - interoperability and extensability

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# ADTV Overview

- **Meeting the FCC schedule with ADTV hardware requires parallel (and cooperative) effort in many ATRC labs:**
  - System design at Sarnoff and TCE-LA
  - Video pre- and post-processing hardware at Sarnoff
  - Motion Estimation hardware at Philips-Paris
  - Compression hardware at Philips-Briarcliff
  - Transport hardware at Sarnoff
  - Tuner and VLD hardware at TCE-Indianapolis

- **Final system integration will be a very difficult and tricky task. We have January and February to make it all work!**

- **The schedule is very aggressive -- there are many elements of risk.**

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# ADTV Overview

- **We also have many parallel efforts within Sarnoff:**
  - Video pre-processor
  - Video post-processor
  - Priority Processor
  - Transport Processor
  - Rate Buffer
  - FEC Encoder
  - Twin-QAM modulation
  - Twin-QAM demodulation and equalizer
  - IF/RF modulation
  - Tuner/IF demodulation
  - Twin-QAM demodulation and equalizer
  - FEC Decoder
  - Inverse Transport Decoder

- **Designing, building, and testing each of these pieces alone is complex...**

- **Pulling it all together requires careful planning**

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# Integration Overview

- **FEC-Modem-RF-Tuner-Modem-FEC (bits to bits)**
- **Priority Processor-Transport-Rate Buffer**
- **Rate Buffer-Inverse Transport-VLD**
- **Entire Transport Subsystem pull-together**
- **Pre-Processor - Post-Processor**

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# What's the Message?

- **Every task is critical**
- **Everyone's contribution is important**
- **Every day counts**
- **We need to carefully monitor our progress**
- **Silently falling behind schedule is not acceptable**
- **Anything we can do to pull up our schedule increases our probability of success!!**

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# This Week's Thank You's

- **Al Acampora - Transport Processor in debug**
  - Rick Bunting, Dave Harris, Rich McCormack
- **Liston Abbott - FEC in debug**
  - Bob Petri, Joe Long
- **Ron Kolczynski - Priority Handler design**
- **Ron Kolczynski - Breakpoint Calculator design**
- **Joe Passe - CodeWord Translator design**
- **Bruce Anderson - ITP design review**
- **Charlie Brooks - Rate Buffer design review (soon)**

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# More Thank You's

- **Ted Wagner - AGC loop**
- **Kevin Kelly - Tuner testing and characterization**
- **Bob Evans - RF frequency translators**
- **Jonathan Schepps - TMS32050 code for equaliser**
- **Jim Palopoli - canceled his vacation**
- **Rich McCormack & Desi McBride - nights &weekends**