

MPEG++ System Design

Sarnoff continued to work on MPEG-2 related issues in preparation for the forthcoming Rome meeting in late Jan. Simulation work is being carried out on the following core experiments: (1) leaky prediction; (2) I-frame motion vectors for concealment; (3) scalable MPEG-2 with cell loss; (4) structured packing. Discussions aimed at harmonizing and/or supporting the transport proposal submitted (in London 11/92) to the MPEG-2 Systems group were held with Philips and Scientific Atlanta.

On a request from FCC's Office of Engineering and technology, Sarnoff and TCE-Indy jointly presented a tutorial on MPEG-2 at Wash. D.C. on Dec. 2.

Work continues on upgrading MPEG2 TM2 compression and system software. The encoder and decoder interfaces have been improved to support scalability features and concealment alternatives. The MPEG-2 system model currently works with one-tier transport software, and is being extended for two-tier operation. The software is being prepared for delivery to TCE-Indy and Hannover in early Feb. 93.

Other specific topics covered during this period include: (i) AD-HDTV tape recording: technical support and encoded bit-streams were provided to two companies collaborating to develop a VTR demonstration; (ii) Multimedia broadcasting with AD-HDTV: work on HRV workstation software and interfaces was started in support of this planned demonstration in 93. (iii) Statistically multiplexed MPEG++: Simulation work on VBR rate control continued, and additional results proving the viability of these techniques have been obtained. (iv) A document describing Comdisco models for the AD-HDTV transmission system has been prepared for TCE-Hannover.

Interference, Coverage area, FCC Allocation Issues:

Assessments of ATTC data for the GI and Zenith/AT&T systems were made. Comparative evaluations of coverage areas were made using the data.

RF Modem Hardware:

Multiple copies of the ATTC hardware, some with minor changes, have been made. Testing of these boards is in progress. These will be used in the shrink and cable regenerative repeater.

Tuners:

Two tuners have been built and are under test. One will be used in the shrink receiver (for two-carrier and single-carrier operation), and the other will be used in the cable regenerative repeater.

The first tuner/down-converter chassis has been assembled and is presently being tested. This is the first of three universal RF receivers that are being built. The 7-inch-high chassis houses the tuner, AGC boards, meter control circuit and power supply in the upper compartment; the lower compartment contains the narrow-band, wide-band and single QAM down-converters, and the symbol-timing circuit. The tuner/down-converters have been configured to accommodate UHF, VHF and cable inputs. This enables the spare tuner/down-converter to be used as a replacement for either system. Another 7-inch-high enclosure will house the synthesizers and crystal oscillators that are needed as local oscillators for the tuner/down-converter. The layout of this enclosure is presently being designed. Most of the synthesizers needed to construct the three oscillator boxes have been assembled and tested. All of the purchased parts have been received, except for a 12 MHz reference oscillator. This oscillator is due in in January.

Final specifications for a new receiver SAW filter were negotiated with the vendor and a purchase order placed. The new filter has 20 db greater stop-band attenuation and 500 KHz narrower passband than the off-the-shelf SAW filter used in the receiver during testing at ATTC and field tests. The narrower passband closes the gap between the upper edge of the SP spectrum and the channel edge. Also the new filter will not require that the IF frequency be offset, thus simplifying the switch over from RF to IF loop-back.

Upgrades to Existing Encoder/Decoder

The original AD-HDTV system, presently installed at NBC in New York City, has been upgraded in anticipation of future value added services and performance improvements. These upgrades include:

A) Bit Serial Data VCR Interface. Connector plates have been installed and appropriately wired in both the SS-QAM Demodulator rack and the Transport Decoder Rack to accommodate combined HP/SP data, clocks, and reference timing for VCR recording and playback.

B) Flexible Services Interface. Connector plates have been installed and appropriately wired in both the Transport Encoder and the Transport

Decoder to access the Auxiliary data channel to support multimedia operation. In addition, an interface board has been designed and installed in the Transport Encoder. This board provides signals to the terminal so that the terminal can have adaptive data rates depending on the buffer occupancy.

C) Trellis Encoder/Decoder Interface. A connector plate and the wiring arrangement between the Transport Encoder rack and the Modulator rack is being designed. The new arrangement will accommodate the additional signals required for Trellis Encoder operation.

D) Trellis Encoder Board Design. The detailed design has been completed. A wire-wrapped board is currently being built with HP and SP channel capability. Programmable ICs have been burned for one channel. A prototype of the convolution encoder portion of the trellis encoder has been tested successfully.

E) Trellis Decoder Board Design. The design (except for the synchronization) has been completed on paper. Three of six programmable IC's have been entered into the computer system. A fourth design is currently being entered. Two designs have been simulated successfully. A board schematic design has been completed. The Viterbi decoder chip along with the microcomputer has been successfully prototype tested (hard decision inputs without noise) in conjunction with the prototype convolution encoder.

F) FEC Encoder. The data scrambler will be synchronized to the block period instead of the current packet period to more adequately scramble the data. Minor changes are being designed to bring out packet-sync, block-sync, and 9-packet timing signals to the back plane for the new Trellis encoder. The design additions and wiring are to be implemented on the primary and backup FEC encoder boards.

G) FEC Decoder - The SP shutdown processing is being re-evaluated to see if any improvement in the transition to HP-only data (in very low CNR operation) is possible.

Byte Serial VCR Interface

A) VCR Nest. The back-plane wiring lists have been generated, and work has begun to provide a card cage to house the boards required to provide a byte serial VCR interface adapter from the bit serial ports described in I A.

B) VCR Input Adapter Board. A new board (FEC Decoder) has been completely fabricated. The board is currently being tested to ensure that it performs correctly as a normal IFEC board. Then the required design changes for specialization as an Input Adapter will be implemented in the Programmable IC's.

C) VCR Output Adapter. A new board (FEC Encoder) has been completely fabricated. The board will be tested to insure that it performs correctly as a normal FEC board. Then the required design changes for specialization as an Output Adapter will be implemented in the Programmable IC's.

Field Test (Shrink) Hardware

A) Nest Design and Fabrication. The nests for the Transport Decoder, the Demodulator and the digital portion of the Post Processor (in the mobile receiver) are completed. The nest wiring lists for the VCR Adapter are completed and the nest is in fabrication. The fabrication of the Demodulator nest in the cable head-end is in progress. Racks to house these components are also being readied.

B) Board Fabrication. The field test unit will use Trellis and FEC designs common to the existing encoder and decoder upgrades described ~~in~~ above. Designs are in progress to incorporate the multiplexer and demultiplexer, required for single carrier QAM operation, into the FEC Encoder and FEC Decoder designs. In addition, several boards in the digital portion of Post Processor, and the Transport Decoder are in fabrication. The analog portion of the Post Processor is complete and has been checked out.